ANALOG DEVICES

# AN-356 APPLICATION NOTE

ONE TECHNOLOGY WAY • P.O. BOX 9106 • NORWOOD, MASSACHUSETTS 02062-9106 • 617/329-4700

## User's Guide to Applying and Measuring Operational Amplifier Specifications

by Ray Stata

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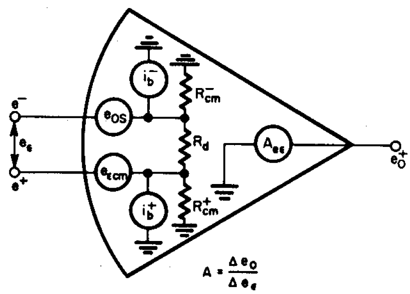


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FIGURE 1. OPERATIONAL AMPLIFIER EQUIVALENT CIRCUIT

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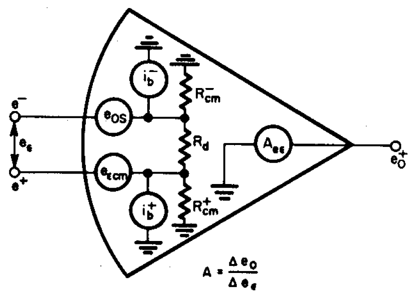


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## UNITY GAIN SMALL SIGNAL RESPONSE

Unity gain small signal response, $f_t$, is the frequency at which the open loop gain becomes unity or zero dB (see figure 2). "Small signal" indicates that in general it is not possible to obtain large output voltage swing at high frequencies because of distortion due to slew rate limiting. Therefore in both measuring $f_t$ and using the amplifier at high frequencies, the output voltage swing must be restricted to avoid slew rate limiting. This implies that the peak output voltage, $e_o$, for a sinusoidal signal at the unity gain frequency, $f_t$, must be less than $S/2\pi f_t$, where S is the slew rate.

For amplifiers with symmetrical response on each input, $f_t$ may be measured by either the inverting circuit of figure 6 or the non-inverting circuit of the figure 7. Some units such as chopper stabilized amplifiers or wideband amplifiers with feed forward design have fast response only on the negative input which restricts testing and use to the inverting circuit. Remember that the closed loop unity gain response of figure 6 will be about one half the open loop unity gain response due to the loading of the feedback network. Moreover, large values of feedback resistance when coupled with stray capacitance may reduce the closed loop response and therefore the smallest possible value of $R_f$ should be used, the limit being set by output current capability $I_o$.

Sometimes $f_t$ is called unity gain-bandwidth product which implies that open loop gain at other frequencies can be predicted from this number. However, gain bandwidth product is constant only for amplifiers with 6dB/octave roll off! For fast roll off amplifiers, gain bandwidth product increases with gain and thus we publish the open loop response curve to give typical gain at each frequency.

## FULL POWER RESPONSE

The large signal and small signal response characteristics of operational amplifiers differ substantially due to dynamic nonlinearities or transient saturation. An amplifier will not respond to large signal changes as fast as the small signal bandwidth characteristics would predict. The most prominent contributor to large signal response limitations is slew rate limiting in the output stages. Circuit and transistor capacitances can be charged and discharged only so fast due to the limited dynamic range of the driving circuits. Transient saturation can also occur in the input stages of the amplifier due to overloading the input stage or due to common mode voltage slew rate limiting, but this is rarely a problem as compared to saturation of the output stages.

Full power response, $f_p$, is the maximum frequency measured at unity closed loop gain, for which rated output voltage, $\pm E_o$, can be obtained for a sinusoidal signal at rated load without distortion due to slew rate limiting. Note that this specification does not relate to "response" in the sense of gain reduction with frequency. Instead it refers only to distortion in the output signal caused by slew rate limiting. For a sinusoidal signal, the maximum slope or rate of voltage change occurs at zero crossing and is proportional to the peak amplitude and the frequency.

Thus we see that to a first approximation slew rate, S, and full power response, $f_p$, are related by equation 1.

$$\left.\frac{de_o}{dt}\right|_{max} = 2\pi f_p E_o = S \qquad \text{(equation 1)}$$

As the voltage swing is reduced below rated output, $E_o$, the operating frequency can be proportionally increased without exceeding the slew rate, S. In the limit the operating frequency approaches the unity gain bandwidth, $f_t$, and the corresponding voltage signal defines the maximum peak amplitude for "small signal" unity gain response. The circuits of figure 6 or figure 7 can be used to measure full power response depending on whether inverting or non-inverting parameters are measured. Where dynamic saturation of the output stages is the primary cause for slew rate limiting either test circuit will give equivalent results. For very fast response amplifiers, load capacitance and/or capacitance from the output to the negative input will cause apparent slew rate limiting and consequent degradation of full power response. This is due to saturation of amplifier output current in charging these capacitances and therefore such capacitances must be low.

Output distortion can be measured either by a distortion meter on the output or by observing a Lissajon pattern on an oscilloscope. There is no industry wide accepted value for the distortion level which determines the full power response limitation, but a number like 1% to 3% is a reasonable figure. One subtle point here is that closed loop output distortion depends on the amount of feedback or loop gain and therefore it depends on the closed loop gain of the measurement. Full power response is generally measured at unity gain where loop gain is the highest. At higher closed loop gains output distortion will increase for the same full power response frequency.



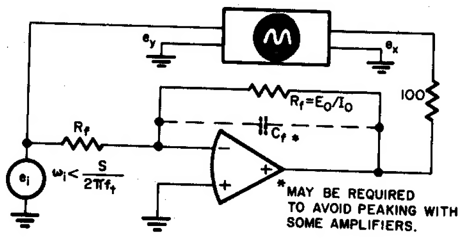


FIGURE 6. INVERTING CIRCUIT FOR MEASURING $f_t$, $f_p$, S, T

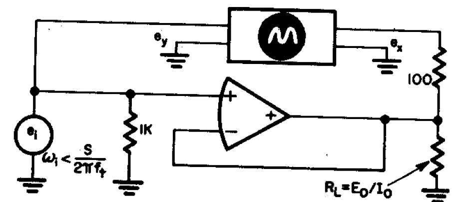


FIGURE 7. NONINVERTING CIRCUIT FOR MEASURING $f_t$, $f_p$, S, T, $E_{cm}$

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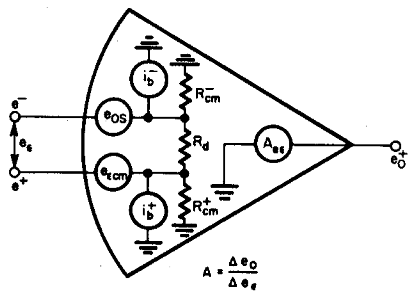


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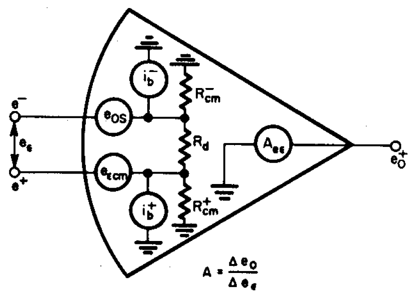


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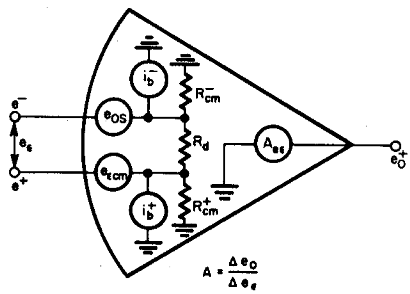


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and adjust $R_s$ for 10% reduction at the output. Then $R_{cm}+=9R_s$. Above this impedance it is advisable to substitute a picoameter for the resistor $R_s$ and to measure DC bias current as a function of common mode voltage.

Common mode impedance is a non-linear function of both temperature and common mode voltage. For FET amplifiers common mode impedance is reduced by a factor of two for each 10°C temperature rise.

As a function of common mode voltage, $R_{cm}$ is defined as average impedance for a common mode voltage change from zero to $\pm E_{cm}$, that is, maximum common mode voltage. Incremental $R_{cm}$ about some large common mode voltage may be considerably less than the specified average $R_{cm}$, especially for FET input amplifiers.

## MAXIMUM VOLTAGE BETWEEN INPUTS

Under most operating conditions, feedback maintains the error voltage, $e_\varepsilon$, between inputs very near to zero volts. However, in some applications, such as voltage comparators, or where the input voltage exceeds the level required to saturate the output, the voltage between inputs can become large. $E_d$ defines the maximum voltage which can be applied between inputs without causing permanent damage to the amplifier. Placing parallel back to back diodes across the input terminals is one way to provide added protection for the amplifier.

## MAXIMUM COMMON MODE VOLTAGE

For differential input amplifiers, the voltage at both inputs can be raised above ground potential. Common mode voltage, $e_{cm}$, is defined as the voltage above ground at each input when both inputs are at the same voltage. $E_{cm}$ is defined as the maximum peak common mode voltage at the input before clipping or excessive non-linearity is seen at the output. $E_{cm}$ establishes the maximum input voltage for the voltage follower connection. (See figure 7.)

$E_{cm}$ is measured with the circuit of figure 7 by increasing the peak input voltage (sinusoidal waveform) until distortion is seen on the scope (about 1 to 3%). The input signal frequency must be well below the full power response frequency, $f_p$, for the non-inverting input.

## COMMON MODE REJECTION

An ideal operational amplifier responds only to the difference voltage between inputs $(e+-e-)$ and produces no output for a common mode voltage — that is when both inputs are at the same potential. However, due to slightly different gains between the plus and minus inputs, common mode input voltages are not entirely substracted at the output. If we refer the output common mode error voltage to the input (dividing by gain) and call this the input common mode error voltage, $e_{\varepsilon_{cm}}$, then common mode rejection (CMR) is defined as the ratio of common mode voltage to common mode error voltage. That is $CMR = e_{cm}/e_{\varepsilon_{cm}}$. CMR is sometimes expressed in dB in which case you take 20 times the log (base 10) of the ratio. Errors due to common mode rejection can be represented in the equivalent circuit of figure 1 by a voltage generator, $e_{\varepsilon_{cm}}$, in series with the input. Note that common mode error goes to zero when either input is grounded. Therefore the inverting configuration does not exhibit a common mode error since the plus input is grounded. Thus CMR is only a problem in the non-inverting and differential configurations where common mode voltage varies in direct proportion to the input signal. In this case $e_{\varepsilon_{cm}}$ is a basic measuring error which affects the overall circuit accuracy.

For example, if a 10 volt signal, $e_i$, were applied to the input of the circuit in Figure 14 common mode voltage, $e_{cm}$, is equal to the input voltage, $e_i$. This would cause a common mode voltage, $e_{\varepsilon_{cm}}$, of 2mV for an amplifier with 5,000 or 74dB CMR and thus a 0.02% measuring error.

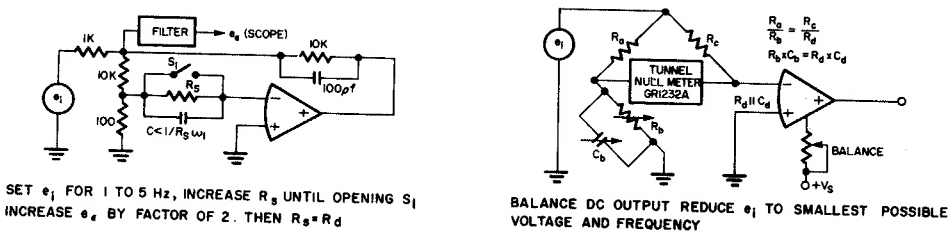
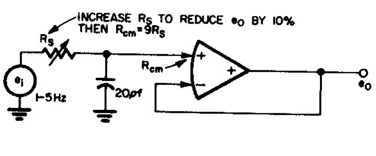



FIGURE 12. DIFFERENTIAL IMPEDANCE TEST CIRCUITS

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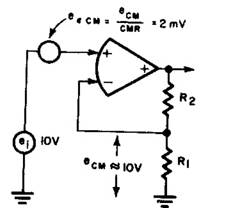


FIGURE 14. ILLUSTRATION OF COMMON MODE VOLTAGE

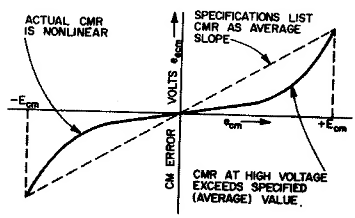


FIGURE 15. CM ERROR VS CM VOLTAGE

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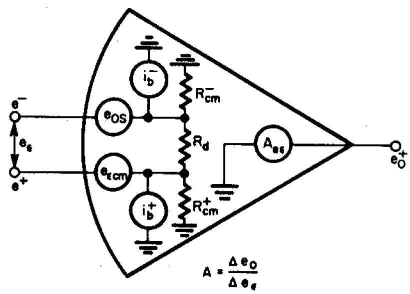


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